

CLAIM AMENDMENTS

1. (Currently Amended) A routing switch having  $(N1+N2)$  input terminals and  $(M1+M2)$  output terminals and comprising:

a first router module having  $N1$  signal input terminals, an expansion input terminal and  $(M1+1)$  output terminals, including  $M1$  signal output terminals and an expansion output terminal, the first router module including a means for routing a signal received at any one of the  $N1$  signal input terminals selectively to any one or more of the  $(M1+1)$  output terminals and for routing a signal received at the expansion input terminal selectively to any one or more of the  $M1$  signal output terminals,

a second router module having  $N2$  signal input terminals, an expansion input terminal and  $(M2+1)$  output terminals, including  $M2$  signal output terminals and an expansion output terminal, the second router module including a means for routing a signal received at any one of the  $N2$  signal input terminals selectively to any one or more of the  $(M2+1)$  output terminals and for routing a signal received at the expansion input terminal selectively to any one or more of the  $M2$  signal output terminals,

input interface circuitry connecting said  $(N1+N2)$  input terminals of the routing switch respectively to the  $N1$  signal input terminals of the first router module and the  $N2$  signal input terminals of the second router module, and

output interface circuitry connecting the  $M1$  signal output terminals of the first router module and the  $M2$  signal output terminals of the second router module to said  $(M1+M2)$  output terminals of the routing switch respectively,

and wherein the expansion output terminal of the first router module is connected to the expansion input terminal of the second router module and the expansion output terminal of the second router module is connected to the expansion input terminal of the first router module,

and the first router module includes a switch core for switching serial digital data streams, the switch core including  $N1$  SIPO registers which convert serial digital data to parallel

form, an input expansion interface for receiving data from the expansion input terminal and providing parallel output data, a memory means which receives and temporarily stores parallel data provided by the N1 SIPO registers and parallel output data provided by the input expansion interface, an output expansion interface connected to the expansion output terminal, M PISO registers connected to the M signal output terminals, and memory output means for selectively providing data read from the memory means to the output expansion interface and the PISO registers.

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omit.

2. (Original) A routing switch according to claim 1, wherein the first router module includes a rectangular crosspoint matrix composed of N1 input conductors connected to the signal input terminals respectively, M1 output conductors connected to the signal output terminals respectively, an input expansion conductor connected to the expansion input terminal, an output expansion conductor connected to the expansion output terminal,  $N1 * M1$  switch elements each operable selectively for connecting a unique combination of one input conductor and one output conductor, N1 switch elements operable selectively for connecting the output expansion conductor to any one of the input conductors and M1 switch elements operable selectively for connecting the output expansion conductor to any one of the M1 output conductors.

RV [ 3. (Cancelled)

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4. (Original) A routing switch according to claim 1, wherein the memory means comprises a first memory which receives and temporarily stores parallel data provided by the N1 SIPO registers and a second memory which receives and temporarily stores parallel output data provided by the input expansion interface, and the memory output means comprises a first intermediate bus, a second intermediate bus, an output bus, a third memory and a fourth memory, and wherein the first

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intermediate bus supplies data from the first memory to the output expansion interface and to the third memory, the second intermediate bus supplies data from both the second memory and the third memory to the fourth memory, and the output bus supplies data from the fourth memory to the PISO registers.

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4/5. (Original) ~~A routing switch according to claim 1,~~ wherein the first router module includes a switch core for switching serial digital data streams, the switch core including N1 SIPO registers which convert serial digital data to parallel form, an input bus which the N1 SIPO registers access sequentially, a first memory which buffers parallel data on the input bus to a first intermediate bus, a second memory which buffers the data on the first intermediate bus to a second intermediate bus, an output expansion interface connected to the first intermediate bus for supplying the parallel data on the first intermediate bus to the expansion input terminal of the second router module, an input expansion interface for receiving data from the expansion output terminal of the second router module and placing the data on the second intermediate bus, a third memory for buffering the data on the second intermediate bus onto an output bus, and M1 PISO registers which access the output bus during selected time slots and converting the parallel data to serial form.

5/4. (Original) A routing switch according to claim 5, wherein the second intermediate bus comprises a first intermediate bus segment and a second intermediate bus segment, the output bus comprises a first output bus segment and a second output bus segment, the second memory comprises a first memory segment for buffering data on the first intermediate bus onto the first intermediate bus segment and a second memory segment for buffering data on the first intermediate bus onto the second intermediate bus segment, and the third memory comprises a first memory segment for buffering data on the first intermediate bus

segment onto the first output bus segment and a second memory segment for buffering data on the second intermediate bus segment onto the second output bus segment.

6/7. (Original) A routing switch according to claim 4, wherein the input expansion interface includes an input expansion bus for receiving data from the second router module and a memory for buffering the data on the input expansion bus onto the second intermediate bus.

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7/6. (Original) A routing switch according to claim 7, wherein the output expansion interface includes a means for converting parallel data on the first intermediate bus to serial form and the input expansion interface includes a means for converting serial data received from the expansion output terminal of the second router module to parallel form.

8/8. (Currently Amended) A router module having N signal input terminals, M signal output terminals, an expansion input terminal and an expansion output terminal and including a router means for routing a signal received at any one of the N signal input terminals to any one or more of the output terminals and for routing a signal received at the expansion input terminal to any one or more of the M signal output terminals, the router means including a switch core for switching serial digital data streams, the switch core including N SIPO registers which convert serial digital data to parallel form, an input bus which reads the N SIPO registers sequentially, a first memory which buffers parallel data on the input bus to a first intermediate bus, a second memory which buffers parallel data on the first intermediate bus to a second intermediate bus, an output expansion interface connected to the first intermediate bus for supplying the parallel data on the first intermediate bus to the expansion output terminal, an input expansion interface for receiving data from the ~~input~~ expansion input terminal and

placing the data on the second intermediate bus, a third memory for buffering the data on the second intermediate bus onto an output bus, and M PISO registers for reading the output bus during selected time slots and converting the parallel data to serial form.

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10. (Currently Amended) A router module having N signal input terminals, M signal output terminals, an expansion input terminal and an expansion output terminal and including a router means for routing a signal received at any one of the N signal input terminals to any one or more of the output terminals and for routing a signal received at the expansion input terminal to any one or more of the M signal output terminals, wherein the router module includes a switch core for switching serial digital data streams, the switch core including N1 SIPO registers which convert serial digital data to parallel form, an input expansion interface for receiving data from the ~~input~~ expansion input terminal and providing parallel output data, a memory means which receives and temporarily stores parallel data provided by the N1 SIPO registers and parallel output data provided by the input expansion interface, an output expansion interface connected to the expansion output terminal, M PISO registers connected to the M signal output terminals, and memory output means for selectively providing data read from the memory means to the output expansion interface and the PISO registers.

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11. (Original) A router module according to claim 10, wherein the memory means comprises a first memory which receives and temporarily stores parallel data provided by the N2 SIPO registers and a second memory which receives and temporarily stores parallel output data provided by the input expansion interface, and the memory output means comprises a first intermediate bus, a second intermediate bus, an output bus, a third memory and a fourth memory, and wherein the first intermediate bus supplies data from the first memory to the

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output expansion interface and to the third memory, the second intermediate bus supplies data from both the second memory and the third memory to the fourth memory, and the output bus supplies data from the fourth memory to the PISO registers.

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12. (Currently Amended) A routing switch comprising  $n$  routers ( $n > 1$ ) and wherein each router comprises  $p$  router modules ( $p \geq 1$ ) each having a plurality of signal input terminals, a plurality of signal output terminals,  $(n-1)$  expansion input terminals and  $(n-1)$  expansion output terminals and including a means for routing a signal received at any one of its signal input terminals to any one or more of its output terminals and for routing a signal received at any one of the expansion input terminals to any one or more of the signal output terminals, and an expansion interconnect network whereby each expansion output terminal of the  $i$ th router module ( $i = 1 \dots p$ ) of the  $j$ th router ( $j = 1 \dots n$ ) is connected to an expansion input terminal of the  $i$ th router module of a router other than the  $j$ th router,

and wherein at least one of the  $p$  router modules includes a switch core for switching serial digital data streams, the switch core including a plurality of SIPO registers which convert serial digital data to parallel form, an input expansion interface means for receiving data from the  $(n-1)$  expansion input terminals and providing parallel output data, a memory means which receives and temporarily stores parallel data provided by the SIPO registers and parallel output data provided by the input expansion interface, an output expansion interface means connected to the  $(n-1)$  expansion output terminals, a plurality of PISO registers connected to the signal output terminals, and memory output means for selectively providing data read from the memory means to the output expansion interface and the PISO registers.

13. (Canceled)